UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/069,805	11/07/2002	Gilbert Wolrich	10559-307US1	7118

7590 03/16/2006

Fish & Richardson
225 Franklin Street
Boston, MA 02110-2804

EXAMINER	
HUISMAN, DAVID J	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 03/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/069,805	WOLRICH ET AL.	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 November 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 November 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *all up to present*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: IDS as received on 2/25/2002, 6/4/2004, 12/4/2004 (x4), and 12/13/2004.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

5. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because the drawings contain text and reference numbers that are illegible. Some of the drawings are also much too small to read. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Rejections - 35 USC § 101

6. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

7. Claims 1-6 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. More specifically, claims 1-6 are directed towards a computer instruction (i.e., software), which is simply an abstract idea. It is not a process, machine, manufacture, or composition of matter.

Claim Objections

8. In claim 1, replace "comprises" with --comprising--.

9. Claim 2 is objected to because it does not end with a period. Appropriate correction is required.

10. Claim 3 is objected to because of the following informalities: Please replace "instruction, ctx" with --instruction and ctx--. Also, replace "the context number" with --the specified context number--. Appropriate correction is required.

11. Claim 4 is objected to because of the following informalities: Please replace "the context number" with --the specified context number--. Appropriate correction is required.

12. Claim 5 is objected to because of the following informalities: Please replace "optional_token" with --optional token--. Appropriate correction is required.

13. Claim 6 is objected to because that grammar is unclear. More specifically, the word "defer" does not appear to belong in the claim, and for purposes of examination, the examiner will ignore the word "defer." Appropriate correction is required.

14. Claim 7 is objected to because of the following informalities: Please replace "comprises" with --comprising-- and "a executing" with --an executing--. Also, replace "an specified" with --a specified--. Appropriate correction is required.

15. Claim 10 is objected to because of the following informalities: Please replace "a executing" with --an executing--. Appropriate correction is required.

16. Claim 13 is objected to because of the following informalities: Please replace "medium" with --storage medium--. Also, replace "a executing" with --an executing--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

17. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

18. Claims 2-4 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. More specifically, the examiner is unclear as to implement and use a branch instruction having the format set forth in

claim 2. That is, why are there two "ctx" fields and what do the brackets represent. The specification and drawings to not appear to explain such a format. In addition,

19. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

20. Claims 2-4 and 6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

21. Regarding claim 2, applicant states that "the instruction has the following format" (i.e., singular), but lists two distinct formats. Clearly, the instruction cannot be of both formats at the same time. Therefore, applicant should clarify the claim so that it is clear that the instruction has "one of the following formats" (any language that makes this clear will be sufficient).

22. Claim 3 recites the limitation "the address branch operation" in the last line of the claim. There is insufficient antecedent basis for this limitation in the claim.

23. Claim 6 recites the limitation "the branch operation" in the last line of the claim. There is insufficient antecedent basis for this limitation in the claim. Is applicant referring to the context branch instruction of claim 5 or to the branch instruction of claim 6 or just some different operation altogether? Also, applicant refers to "the instruction" in line 2 of the claim. Is applicant referring to the context branch instruction following another branch instruction or to a second instruction following the context branch instruction? Applicant must take the appropriate steps to clarify the claim. The examiner's interpretation of the claim for purposes of examination will be evident below.

Claim Rejections - 35 USC § 102

24. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

25. Claims 1-3, 7-8, 10-11, and 13-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Eickemeyer et al., U.S. Patent No. 6,061,710 (herein referred to as Eickemeyer).

26. Referring to claim 1, Eickemeyer has taught a computer instruction comprises a context branch that causes an instruction stream to branch to another instruction stream having an address at a specified label based on whether or not a current context number matches a specified context number. See Fig.2, Fig.5, and column 6, line 25, to column 7, line 16. Essentially, a branch instruction will try to reserve/specify a hardware context so that the alternate branch path may be executed on that context (Fig.2 shows a signal for reserving context N for the alternate branch leg). If that context N is available (i.e., context N is the current context), then the branch will occur and the alternate/target path will be executed. However, if context N is unavailable, then the current context is not context N, and the alternate/target path may not be selected for execution. In addition, a target address (label) must clearly be specified by the branch.

27. Referring to claim 2, Eickemeyer has taught a context branch instruction as described in claim 1. Eickemeyer has further taught that the instruction has the following format: br=ctx[ctx,label#], optional_token, br!=ctx[ctx,label#], optional_token. In a first interpretation

of the claim, the examiner assumes that the branch instruction may be either one of the formats since it cannot be both at the same time. And, since the token is optional, the first format could be seen to cover "br=ctx[ctx, label#], token" or "br=ctx[ctx, label#]". The examiner asserts that Eickemeyer teaches the latter in that the branch will specify a context to reserve as well as an address. Eickemeyer does not mention anything about a token in the branch instruction, but since applicant's token is optional, Eickemeyer does not need to have this token.

28. Referring to claim 3, Eickemeyer has taught a context branch instruction as described in claim 1. Eickemeyer has further taught that the label# is a symbolic label corresponding to the address of an instruction, ctx is the context number. As discussed above, Eickemeyer's branches will specify a context to reserve and also an branching address.

29. Referring to claim 7, Eickemeyer has taught a method of operating a processor comprises evaluating a context number of an executing context to determine whether the context number of the executing context matches a specified context number, and branching to a specified instruction in accordance with evaluating the context number of the executing context. See Fig.2, Fig.5, and column 6, line 25, to column 7, line 16. Essentially, a branch instruction will try to reserve/specify a hardware executing context (a context associated with execution) so that the alternate branch path may be executed on that context (Fig.2 shows a signal for reserving context N for the alternate branch leg). If that context N is available, then the branch will occur and the alternate/target path will be executed.

30. Referring to claim 8, Eickemeyer has taught a method as described in claim 7. Eickemeyer has further taught that branching further comprises branching if the executing context number matches the specified context number. As previously explained, a context will

be specified via signal shown in Fig.2, and if the executing context is available, branching occurs, and the alternate path will be executed.

31. Referring to claim 10, Eickemeyer has taught a processor that can execute multiple contexts and that comprises:

a) a register stack. See column 8, lines 43-63 and note that each context has a separate register pool.

b) a program counter (PC) for each executing context. See column 8, lines 43-63, and note that each context receives a PC.

c) an arithmetic logic unit coupled to the register stack (an ALU inherently exists to execute arithmetic/logical type operations) and a program control store that stores a context swap instruction (branch instruction) that causes the processor to evaluate a context number of an executing context to determine whether the context number of the executing context matches a specified context number, and branch to a specified instruction in accordance with evaluating the context number of the executing context. See Fig.2, Fig.5, and column 6, line 25, to column 7, line 16. Essentially, a branch instruction will try to reserve/specify a hardware executing context (a context associated with execution) so that the alternate branch path may be executed on that context (Fig.2 shows a signal for reserving context N for the alternate branch leg). If that context N is available, then the branch will occur and the alternate/target path will be executed.

32. Referring to claim 11, Eickemeyer has taught a processor as described in claim 10. Furthermore, claim 11 is rejected for the same reasons set forth in the rejection of claim 8.

33. Referring to claim 13, Eickemeyer has taught a computer program product residing on a computer-readable medium (see Fig.1, components 130, 140, and 150, for instance) for causing a

processor that executes multiple contexts to perform a function comprises instructions causing the processor to evaluate a context number of an executing context to determine whether the context number of the executing context matches a specified context number, and branch to a specified instruction in accordance with evaluating the context number of the executing context. See Fig.2, Fig.5, and column 6, line 25, to column 7, line 16. Essentially, a branch instruction will try to reserve/specify a hardware executing context (a context associated with execution) so that the alternate branch path may be executed on that context (Fig.2 shows a signal for reserving context N for the alternate branch leg). If that context N is available, then the branch will occur and the alternate/target path will be executed.

34. Referring to claim 14, Eickemeyer has taught a product as described in claim 13. Furthermore, claim 14 is rejected for the same reasons set forth in the rejection of claim 8.

Claim Rejections - 35 USC § 103

35. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

36. Claims 2-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eickemeyer, as applied above, in view of Dowling, U.S. Patent No. 6,157,988.

37. Referring to claim 2, Eickemeyer has taught a context branch instruction as described in claim 1. Eickemeyer has further not taught that the instruction has the following format: br=ctx[ctx,label#], optional_token, br!=ctx[ctx,label#], optional_token. The prior art only needs

to teach one of these formats to anticipate the claim. Eickemeyer does teach inherently teach a general format of br=ctx[ctx,label#] because the branch in Eickemeyer will specify a context to reserve and also provide a branching address. Using a second interpretation of the claim, Eickemeyer does not specifically teach a field for holding an optional token. However, Dowling has taught such a concept. See column 16, lines 43-54 and note that a branch instruction may have a field for holding a token that specifies whether or not the branch is early-resolvable. By tracking this, branches may be resolved one cycle earlier. As a result, in order to increase the speed of processing branches, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Eickemeyer such that the branch includes an optional token.

38. Referring to claim 3, Eickemeyer in view of Dowling has taught a context branch instruction as described in claim 1. Eickemeyer has further taught that the label# is a symbolic label corresponding to the address of an instruction, ctx is the context number. As discussed above, Eickemeyer's branches will specify a context to reserve and also an branching address.

39. Referring to claim 4, Eickemeyer in view of Dowling has taught a context branch instruction as described in claim 3. While Eickemeyer has not explicitly taught that the context number has valid values of 0, 1, 2, or 3, Eickemeyer has taught that there are "n" contexts. See Fig.2. Clearly, it makes the most sense to number the contexts starting with 0, mainly because this would ensure that the least number of bits would be used to address the contexts. For instance, assume there are 15 contexts. If we start numbering the contexts with 0, then the system would need four address bits to address any of the 15 contexts (since we'd be addressing contexts 0-14 (0000-1110 in binary)). However, if we start numbering the contexts at 4, then we would need 5 bits to perform addressing (since we'd be addressing contexts 4-18 (00100-10010

in binary)). As a result, it would have been obvious for valid contexts to include 0, 1, 2, or 3 since it Eickemeyer has said that there are "n" contexts and it makes the most sense to have "n" include 0, 1, 2, etc.

40. Referring to claim 5, Eickemeyer has taught a computer instruction as described in claim 1. Eickemeyer has not taught that the instruction has an optional token. However, Dowling has taught such a concept. See column 13, lines 14-20, and 16, lines 43-54, and note that a branch instruction may have a field for holding a token that specifies whether or not the branch is early-resolvable. By tracking this, branches may be resolved one cycle earlier. As a result, in order to increase the speed of processing branches, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Eickemeyer such that the branch includes an optional token.

41. Claims 4, 9, 12, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eickemeyer, as applied above.

42. Referring to claim 4, Eickemeyer in view of Dowling has taught a context branch instruction as described in claim 3. While Eickemeyer has not explicitly taught that the context number has valid values of 0, 1, 2, or 3, Eickemeyer has taught that there are "n" contexts. See Fig.2. Clearly, it makes the most sense to number the contexts starting with 0, mainly because this would ensure that the least number of bits would be used to address the contexts. For instance, assume there are 15 contexts. If we start numbering the contexts with 0, then the system would need four address bits to address any of the 15 contexts (since we'd be addressing contexts 0-14 (0000-1110 in binary)). However, if we start numbering the contexts at 4, then we

would need 5 bits to perform addressing (since we'd be addressing contexts 4-18 (00100-10010 in binary)). As a result, it would have been obvious for valid contexts to include 0, 1, 2, or 3 since it Eickemeyer has said that there are "n" contexts and it makes the most sense to have "n" include 0, 1, 2, etc.

43. Referring to claim 9, Eickemeyer has taught a method as described in claim 7. Furthermore, claim 9 is rejected for the same reasons set forth in the rejection of claim 4 above.

44. Referring to claim 12, Eickemeyer has taught a processor as described in claim 10. Furthermore, claim 12 is rejected for the same reasons set forth in the rejection of claim 9 above.

45. Referring to claim 15, Eickemeyer has taught a processor as described in claim 14. Furthermore, claim 15 is rejected for the same reasons set forth in the rejection of claim 9 above.

46. Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eickemeyer, as applied above, in view of Holmann, et al., U.S. Patent No. 5,815,698 (herein referred to as Holmann).

47. Referring to claim 5, Eickemeyer has taught a context branch instruction as described in claim 1. Eickemeyer has not taught that the instruction has an optional token. However, Holmann has taught such a concept. See Fig.13-17 and column 13, lines 56-59, and note the delay field. The delay field holds a variable amount of delay until the branch is executed. So, an amount of instructions equal to the delay amount and following the branch may begin executing. This has the well known advantage of not sitting idle while the processor waits to determine the outcome of the branch. Consequently, it would have been obvious to one of ordinary skill in the

art at the time of the invention to modify Eickemeyer such that the branch includes an optional token (delay amount).

48. Referring to claim 6, Eickemeyer in view of Holmann has taught a context branch instruction as described in claim 5. Eickemeyer in view of Holmann, for the reasons discussed in the rejection of claim 5 above, has further taught that the instruction has an optional token that causes a processor to execute the instruction following the branch instruction before performing the branch operation.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
March 8, 2006

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100